ECE 120 Second Midterm Exam
Fall 2017

Tuesday, October 24, 2017

Name: _____ NetID: _____

Discussion Section and TA Name:

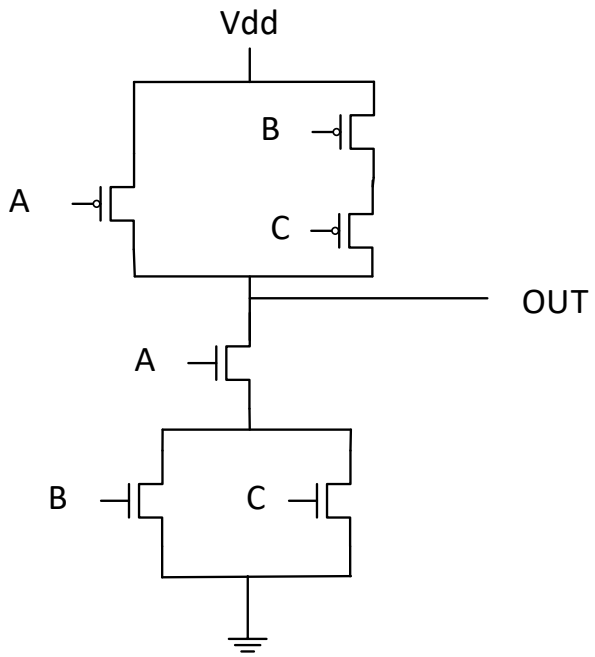
11:00 AM	[ ] AD1 Ruby	[ ] AD8 Matt
12:00 PM	[ ] AD2 David	[ ] AD9 Matt
1:00 PM	[ ] AD3 David	[ ] ADA Yu-Hsuan
2:00 PM	[ ] AD4 Wanzheng	[ ] ADB Zhaoheng
3:00 PM	[ ] AD5 Wanzheng	
4:00 PM	[ ] AD6 Spencer	[ ] ADC Ruby
5:00 PM	[ ] AD7 Spencer	[ ] ADD Zhaoheng

- **Be sure that your exam booklet has 8 pages.**
- **Write your name and netid and check your discussion section on this page.**
- **Do not tear the exam booklet apart, except for the last page.**
- **Use backs of pages for scratch work if needed.**
- **This is a closed book exam. You may not use a calculator.**
- **You are allowed one handwritten 8.5 x 11" sheet of notes (both sides).**
- **Absolutely no interaction between students is allowed.**
- **Clearly indicate any assumptions that you make.**
- **The questions are not weighted equally. Budget your time accordingly.**
- **Show your work.**

Problem 1	16 points	_____
Problem 2	17 points	_____
Problem 3	16 points	_____
Problem 4	17 points	_____
Problem 5	18 points	_____
Problem 6	16 points	_____
Total	100 points	_____

Problem 1 (16 points): CMOS Gates and Truth Tables

1. **(8 points)** Fill in the truth table **with 0s and 1s only** for the CMOS circuit below.



A	B	C	OUT
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

2. **(8 points)** You will help design a circuit that converts a 3-bit two's complement number $T_2T_1T_0$ into a 2-bit unsigned number U_1U_0 with the same magnitude. For example:

If $T_2T_1T_0$=111 then U_1U_0=01

Use **don't cares** if you cannot represent the magnitude as a 2-bit unsigned number. Describe your circuit as a truth table below. One row has been provided for you.

T_2	T_1	T_0	U_1	U_0
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1	0	1

Problem 2 (17 points): Simplification with Don't Cares and 2-level Design

1. Consider the 4-variable function **E(A,B,C,D)**, with the following K-map (drawn twice). **Note:** there are extra copies of this K-map on the last page of the exam. Use them for scratch work, but they will **not** be graded. Make sure to mark the two K-maps below correctly.

Minimal SOP

E(A,B,C,D)	AB			
CD	00	01	11	10
00	1	1	0	1
01	0	1	1	X
11	0	X	X	0
10	0	0	0	0

Minimal POS

E(A,B,C,D)	AB			
CD	00	01	11	10
00	1	1	0	1
01	0	1	1	X
11	0	X	X	0
10	0	0	0	0

a. **(6 points)** Give a **minimal SOP** expression for **E(A,B,C,D)** and show the corresponding loops on the **left map**.

Minimal SOP: **E(A,B,C,D) =** _____

b. **(6 points)** Give a **minimal POS** expression for **E(A,B,C,D)** and show the corresponding loops on the **right map**.

Minimal POS: **E(A,B,C,D) =** _____

2. **(5 points)** The function **G(W,X,Y,Z) = W'(Y+Z')(X+Y'+Z)** is in minimal POS form. Draw the implementation of this function as a 2-level circuit using NOR gates only. Use as few NOR gates as possible for full credit. **Assume complemented inputs are available. Clearly label all signals.**

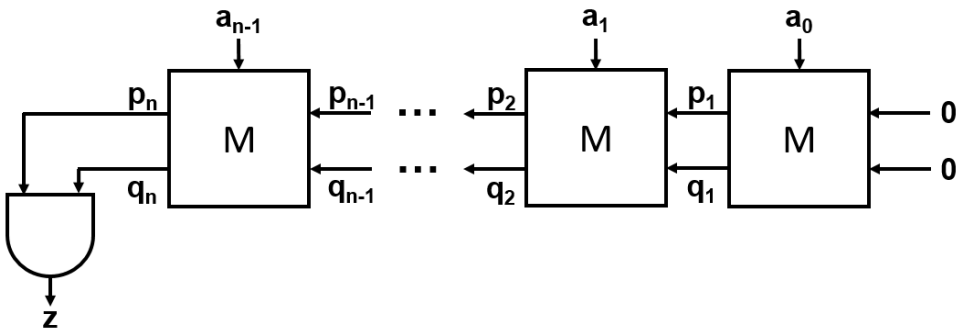
Problem 3 (16 points): Bit-Sliced Design

Let A = a_{n-1} ... $a_2a_1a_0$ be an **n-bit** input.

Design a circuit which outputs **z = 1** if A contains **exactly two 1s**. For example, for n = 5:

- if A = 10010, then z = 1
- if A = 00100, then z = 0
- if A = 01111, then z = 0

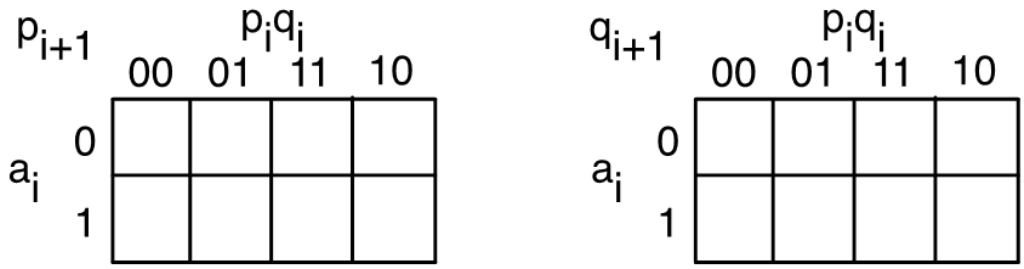
Your implementation should use the bit-sliced design shown below. Each identical copy of network M has inputs a_i, p_i and q_i, and has outputs p_{i+1} and q_{i+1}.



1. **(8 points)** Give meanings to each combination of the carry bits $p_{i+1}q_{i+1}$ in the table below, so that they are **consistent with the diagram above**. One meaning has been provided to you.

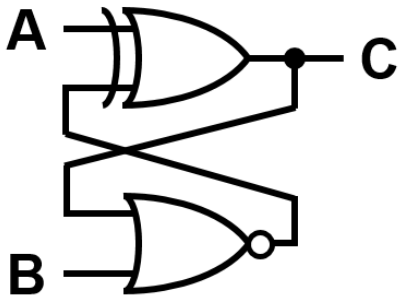
p_{i+1}	q_{i+1}	Meaning
0	0	
0	1	Exactly one 1 has been seen so far
1	0	
1	1	

2. **(8 points)** Fill in the K-maps below for p_{i+1} and q_{i+1}.



Problem 4 (17 points): Sequential Feedback Circuits and Decoders

1. **(9 points)** Circle **all correct answers** to the following questions about the circuit shown on the right. **Note:** there are extra copies of this circuit on the last page of the exam. Use them for scratch work, but they will **not** be graded.



   Which inputs AB force the output C to a steady value of 0 regardless of the initial value of C?

   00 01 10 11 None

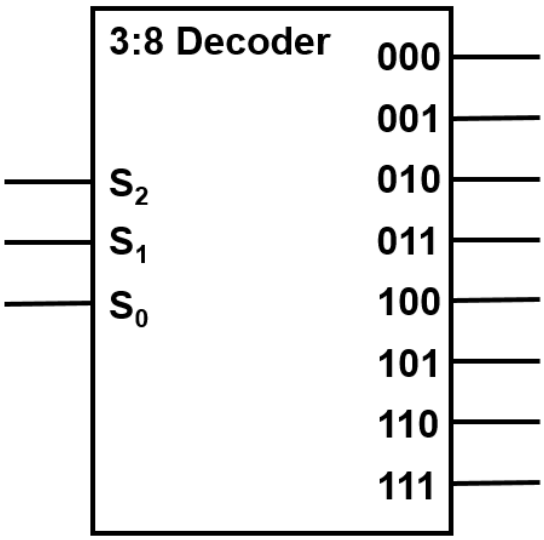
   Which inputs AB force the output C to a steady value of 1 regardless of the initial value of C?

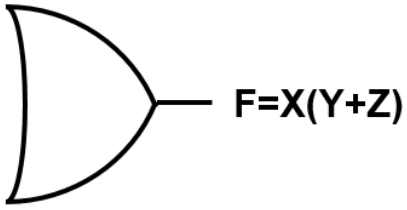
   00 01 10 11 None

   Which inputs AB make the output C switch between 0 and 1 indefinitely?

   00 01 10 11 None

2. **(8 points)** Implement the Boolean function **F = X(Y+Z)** using the 3:8 decoder (without enable input) shown below. Label all inputs to the decoder and connect the decoder to the OR gate using **wires only**. **You may not add any components nor any additional gates.** Complemented inputs are **not** available.



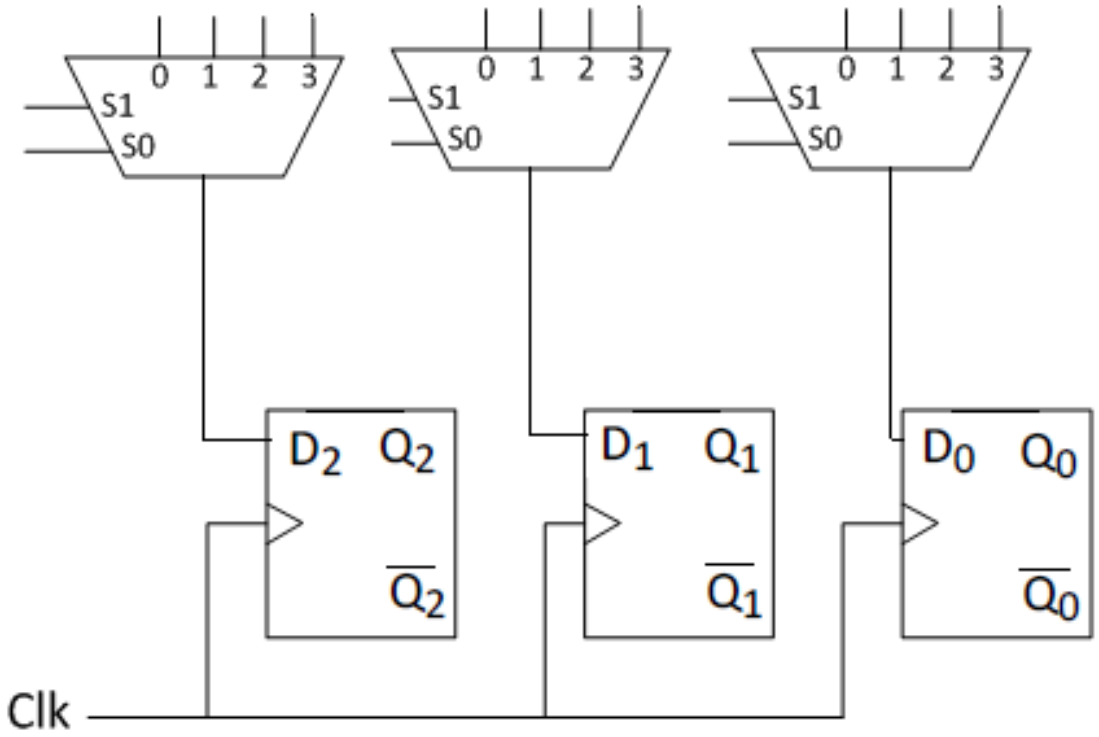


Problem 5 (18 points): Registers

Consider a 3-bit shift register that has the functionality specified in the table to the right.

A	B	Operation
0	0	Hold value
0	1	Flip all bits
1	0	Arithmetic shift right
1	1	Logical shift left

1. **(14 points)** Label the inputs to the muxes to complete the design of this 3-bit register that performs the operations listed in the table. **Use labels and do not draw any additional gates or wires**.



2. **(2 points)** If the shift register initially stores $Q_2Q_1Q_0$=101, what is stored in the register after one clock cycle when AB=10?

   Answer: $Q_2Q_1Q_0$=_____

3. **(2 points)** If the shift register initially stores $Q_2Q_1Q_0$=000, and in the next clock cycle, the register has the values $Q_2Q_1Q_0$=000, which of the following operations could the register be implementing? **Circle ALL possible answers.**

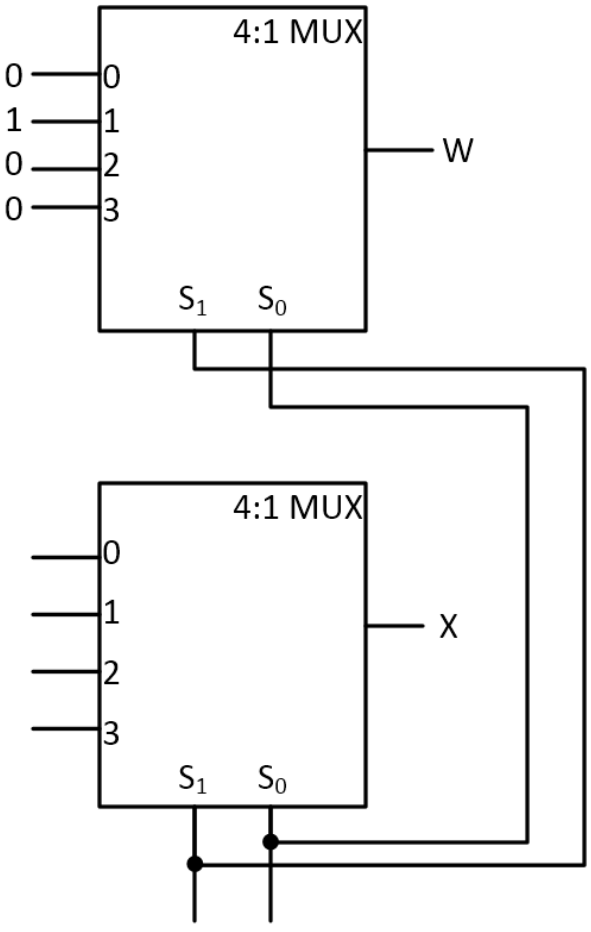
   Hold value Flip all bits Arithmetic shift right Logical shift left

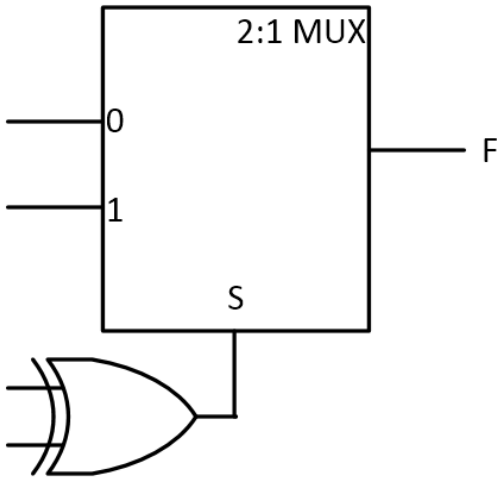
Problem 6 (16 points): Designing Logic with Components

Label the inputs to the muxes and the logic gate provided below to complete the design of the 4 variable function *F* given by the truth table to the right. If you need to refer to the outputs of the muxes or the logic gate, use the names we have specified in the diagram.

Use labels and do not draw any additional gates or wires. Complemented inputs are NOT available.

Variables				Function
A	Z	D	G	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0





Extra copies of K-map for problem 2 (use as scratch copies, we will NOT grade them)

E(A,B,C,D)

CD \ AB	00	01	11	10
00	1	1	0	1
01	0	1	1	X
11	0	X	X	0
10	0	0	0	0

E(A,B,C,D)

CD \ AB	00	01	11	10
00	1	1	0	1
01	0	1	1	X
11	0	X	X	0
10	0	0	0	0

E(A,B,C,D)

CD \ AB	00	01	11	10
00	1	1	0	1
01	0	1	1	X
11	0	X	X	0
10	0	0	0	0

E(A,B,C,D)

CD \ AB	00	01	11	10
00	1	1	0	1
01	0	1	1	X
11	0	X	X	0
10	0	0	0	0

Extra copies of circuit for problem 4 (use as scratch copies, we will NOT grade them)